EXPERIMENT D11: SEQUENTIAL LOGIC CIRCUITS

Related course: KIE1003 (Digital System)

OBJECTIVES:

1. To construct flip-flop circuits using basic logic gates.
2. To construct sequential circuits using flip-flops.

EQUIPMENT / MATERIALS:

DC power supply; breadboard; wires/jumpers; logic gate ICs: 74XX08, 74XX02, 74XX04, 74XX32 (XX can be HC, LS or AC); D flip-flop IC: 74XX74; LEDs; 470Ω and 1kΩ resistors

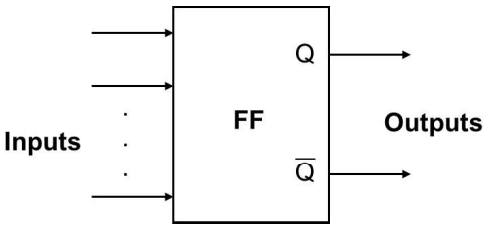
INSTRUCTIONS:

1. Record all your results and observations in a logbook or on a piece of paper.
2. Follow the demonstrator's instructions throughout the experiment.
3. Make sure that the DC power supply is **switched OFF** before connecting and disconnecting the circuit.
4. **Place/remove every IC on/from the breadboard carefully** to avoid pin damage.
5. Please refer to the datasheets for the pin configuration of the logic gate ICs.

INTRODUCTION

Flip-flop (latch) is an important memory element made of an assembly of logic gates. Several different gate arrangements are used to produce flip-flops. Hence, the concept of feedback is important to connect certain gate outputs back to the appropriate gate inputs. This is to allow the connected gates to store information, which is the main function of a flip-flop.

Refer to Figure A to understand the general symbol used in representing a flip-flop. Q is the normal flip-flop output, while its inverse, $\overline{Q}$, is the inverted flip-flop output. Whenever we refer to the state of a flip-flop, we are referring to the state of its normal (Q) output. Note that Figure A implies that a flip-flop can have more than one inputs to cause the flip-flop to switch back and forth ("flip flop") between its output possible states.



Q = 1, $\overline{Q}$ = 0	called HIGH or '1' state also called SET state
Q = 0, $\overline{Q}$ = 1	called LOW or '0' state also called RESET state

Figure A: Symbol of a flip-flop (FF) and its states

There are two possible operating states for a flip-flop. The HIGH or 1 state (Q = 1, $\overline{Q}$ = 0) is also referred to as the **SET** state. Whenever the inputs to a flip-flop cause it to go to the Q = 1 state, we call this setting the flip-flop; the flip-flop has been set. In a similar way, the LOW or 0 state (Q = 0, $\overline{Q}$ = 1) is referred to as the **CLEAR** or **RESET** state.

PROCEDURE:

TEST 1: Gated SR Latch

1. Referring to Figure 1, construct a gated SR latch circuit using NOR gate IC (74XX02) and AND gate IC (74XX08) on a breadboard.

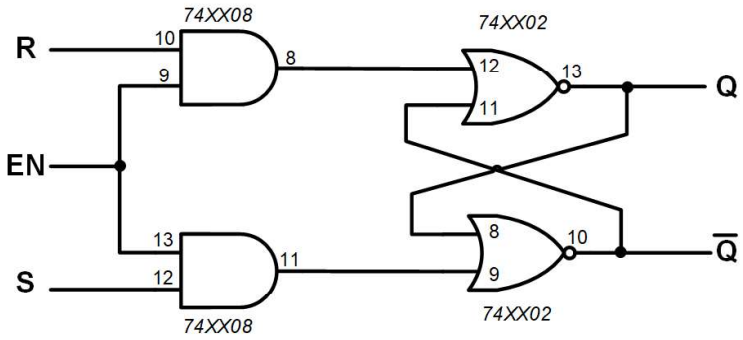


Figure 1

2. Connect V_{CC} (pin 14) of every IC to +5V through a 470Ω resistor and GND (pin 7) to 0V of the DC power supply. Connect the outputs to LEDs.
3. Switch ON the DC power supply. Take a photo of your circuit.
4. Connect the input by following the sequence shown in Table 1. Make sure that you connect/disconnect E first before connecting/disconnecting R and S. For example:
   - When EN=1, R=1 or S=1, that means it is connected to +5V.
   - When EN=0, R=0 or S=0, that means it is connected to 0V.
5. For every combination of inputs, record the output in Table 1, where:
   - When the LED is ON, that means the output Q = 1 or $\overline{Q}$= 1.
   - When the LED is completely OFF, that means the output Q = 0 or $\overline{Q}$= 0.
6. Switch OFF the DC power supply.

Table 1

Input			Output	
EN	**R**	**S**	**Q**	**$\overline{Q}$**
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

TEST 2: D Flip-Flop

1. Using the 74XX74 IC, construct the circuit shown in Figure 2 on a breadboard.
2. Connect all inputs (D, CLK, PRE and CLR) to pushbuttons and all outputs to LEDs.
3. Switch ON the DC power supply. Proceed through the conditions in Table 2 and record the results accordingly.

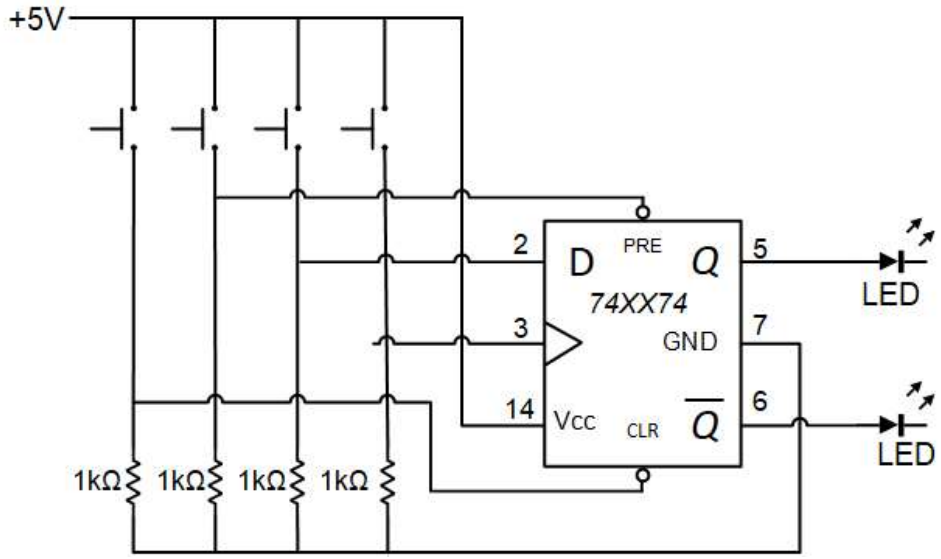


Figure 2

Table 2

Input				Output	
$\overline{PRE}$	$\overline{CLR}$	D	CLK	Q	$\overline{Q}$
0	1	X	X		
1	0	X	X		
0	0	X	X		
1	1	0	↑		
1	1	1	0		
1	1	1	↑		
1	1	0	0		
1	1	0	↑		

DISCUSSION:

1. Explain the operation of gated SR latch.
2. Explain the operation of D flip-flop. Determine whether the flip-flop you are using a positive edge triggered or a negative edge triggered.
3. Explain the difference between gated latch and flip-flop.

OPEN-ENDED TASK:

The process of converting a D flip-flop into a JK flip-flop is initiated by obtaining a table that represents both the information present in the truth table of the JK flip-flop and the information conveyed by the excitation table of the D flip-flop. Complete the D-to-JK conversion table in Table 3 and construct a JK flip-flop circuit using logic gates and D flip-flop only. Include the schematic drawing, calculations (such as Karnaugh map and Boolean expression) and photo of the logic circuit in your report.

Table 3

JK Inputs		Outputs		D input
J	**K**	**Present state, Q_n**	**Next state, Q_{n+1}**	**D**
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0			
1	0			
1	1			
1	1			

END OF EXPERIMENT