STUDENT LAB SAFETY, HIRARC, DATASHEET VERIFICATION CHECKLIST, AND BRIEF REPORT SUBMISSION

EXPERIMENT E12: KIRCHHOFF'S CIRCUIT LAWS

STUDENT NAME : _____
MATRIC NO. : _____
GROUP : _____
DATE : _____

A. Equipment and Measurement Verification Checklist

Item	Verification Requirement	✓
DC Power Supply	Output voltage verified at +5 V DC	
DC Power Supply	Output polarity verified	
Multimeter	Measurement mode (Voltage / Current / Resistance) selected correctly	
Multimeter	Correct terminals used for voltage and current measurements	
Breadboard	No damaged contacts or loose connections	
Resistors	Resistance values verified before use	
Circuit Wiring	Connections checked against Figure 1	
Circuit Wiring	Connections checked against Figure 2	
Current Measurement	Ammeter connected in series before measurement	
Voltage Measurement	Voltmeter connected in parallel before measurement	
Theoretical Calculations	Pre-lab KCL and KVL calculations completed	

B. HIRARC Checklist

Hazard / Unsafe Condition	Potential Consequence	Control Measure	✓
Incorrect power-supply polarity	Circuit malfunction or component damage	Verify polarity before energising	
Incorrect multimeter mode selection	Meter fuse damage or inaccurate readings	Verify measurement mode before connection	
Ammeter connected in parallel	Short circuit and meter damage	Ensure current measurements are performed in series	
Voltmeter connected in series	Incorrect readings and circuit disruption	Ensure voltage measurements are performed in parallel	
Incorrect resistor value used	KCL/KVL verification errors	Verify resistor values before circuit assembly	

Short circuit on breadboard	Excessive current and component damage	Inspect wiring before power ON	
Measuring resistance on an energized circuit	Meter damage and inaccurate measurements	Disconnect power before resistance measurement	
Touching probe tips during resistance measurements	Inaccurate resistance readings	Hold only insulated probe handles	
Modifying circuit while energized	Component damage and measurement errors	Switch OFF power before modifications	
Incorrect recording of data	Invalid verification of KCL and KVL	Verify measurements before submission	

C. Engineering Practice Verification

Requirement	✓
Theoretical calculations completed before laboratory session	
Actual resistor values measured and recorded	
Correct measurement techniques used for voltage and current	
Circuit independently checked before energising	
Experimental values compared with theoretical values	
KCL verification completed using measured currents	
KVL verification completed using measured voltages	
Measurement uncertainties and errors considered	
Results recorded accurately and honestly	
Circuit modifications performed only with power OFF	

D. Student Declaration

I confirm that:
☐ Theoretical KCL and KVL calculations have been completed.
☐ Resistor values have been measured and verified.
☐ Multimeter settings have been checked before measurements.
☐ Voltage measurements will be performed in parallel.
☐ Current measurements will be performed in series.
☐ Circuit connections have been verified against the laboratory schematic.
☐ Hazards have been identified and appropriate control measures implemented.
☐ No damaged equipment or components are being used.
☐ Demonstrator approval has been obtained before energising the circuit.

Student Signature : _____
Date : _____

E. Experiment Data Results and Discussion

In Lab TASK

Test 1: Kirchhoff's Current and Voltage Law (KCL, KVL)

Resistor	Theoretical Resistance ($R_{theoretical}$)	Measured Resistance ($R_{measured}$)
R_1	100 Ω	
R_2	220 Ω	
R_3	100 Ω	
R_4	220 Ω	
R_5	150 Ω	
R_6	50 Ω	

Current	Theoretical current from measured resistance (I)	Experimental measured Current (I)	% Error
	I_1 =	I_1 =	
	I_2 =	I_2 =	
KCL at Node A	I_3 =	I_3 =	
	I_3 =	I_3 =	
	I_4 =	I_4 =	
KCL at Node B	I_5 =	I_5 =	

Verification of KCL from experimental	
KCL at Node A	I_1 = _____, $I_2 + I_3$ = _____
KCL at Node B	I_3 = _____, $I_4 + I_5$ = _____

Theoretical Voltage (V)	Measured Voltage (V)	Verification of KVL
V_{R1} =		
V_{R2} =		
V_{R3} =		
V_{R4} =		
V_{R5} =		
V_{R6} =		

KVL Loop	Derivation	Verification
SAGS		
ABGA		
SABGS		

Test 2: Special Circuit

Measurement	Value	Comments
R		
V_{EB}		
I_{EB}		
Input Resistance		

Voltage Measurement	Measured Value	Comments
B and C		
B and D		
C and D		

Condition	Measured Current (I_{EB})	Comments
R between C and D is removed and a wire is inserted.		
R between C and D is removed (open circuit).		

DISCUSSION:

CONCLUSION:

LAB LECTURER
SIGNATURE : _____

DATE : _____

INSTRUCTOR
SIGNATURE : _____

DATE : _____