STUDENT LAB SAFETY, HIRARC, DATASHEET VERIFICATION CHECKLIST, AND BRIEF REPORT SUBMISSION

Experiment PCB1: PCB Layout Design 1

STUDENT NAME : _____
MATRIC NO. : _____
GROUP : _____
DATE : _____

A. Software and Design Verification Checklist

Item	Verification Requirement	✓
EazyEDA	Simulation Mode selected	
Project Setup	New project created and saved	
Schematic	Circuit schematic completed according to Circuit 1	
Components	Op-amp, resistors, capacitors, power supplies correctly selected	
Component Values	Design values assigned and documented	
Ground Node	Ground connection inserted correctly	
Wiring	All component connections verified	
Power Supply	±VCC values assigned to op-amp	
AC Source	Input source set to 1 Vpp, 1 kHz	
AC Analysis	Frequency sweep set from 10 Hz to 1 MHz	
Measurement Probe	Output node selected correctly	
Simulation Settings	AC analysis configured correctly	
Bode Plot	Gain and phase response generated successfully	
Project File	Saved for use in PCB Layout Design 2	

B. HIRARC Checklist

Hazard / Unsafe Condition	Potential Consequence	Control Measure	✓
Incorrect component selection	Invalid circuit operation and simulation results	Verify component type and datasheet before simulation	
Incorrect component values	Incorrect gain and frequency response	Verify values before simulation	
Missing power-supply connection	Circuit fails to operate	Check all op-amp supply connections	

Missing ground reference	Simulation failure	Confirm circuit contains a valid ground node	
Incorrect wiring connection	Invalid simulation results	Cross-check schematic before analysis	
Incorrect AC-analysis settings	Incorrect Bode plot response	Verify frequency range and simulation parameters	
Failure to save project files	Loss of design work	Save and back up project files regularly	
Poor workstation ergonomics	Eye strain and fatigue	Maintain proper posture and take short breaks	
Data recording errors	Incorrect engineering conclusions	Verify gain and phase data before reporting	
Data manipulation or fabrication	Violation of engineering ethics	Report actual simulation results only	

C. Engineering Practice Verification

Requirement	✓
Op-amp datasheet reviewed before design	
Component values justified and documented	
Schematic independently verified before simulation	
Input-source parameters checked	
Bode plot results reviewed critically	
Simulation results compared with theoretical calculations	
Gain calculations verified	
Design files saved and backed up	
Results recorded accurately and honestly	
Design prepared for subsequent PCB layout stage	

D. Student Declaration

I confirm that:
☐ The circuit schematic has been verified before simulation.
☐ Component values and power-supply requirements have been checked.
☐ AC analysis settings comply with the laboratory requirements.
☐ The Bode plot has been generated using verified simulation parameters.
☐ Simulation results will be compared with theoretical calculations.
☐ Project files have been saved and backed up.
☐ Hazards associated with software-tool usage and data integrity have been identified.
☐ Reported results represent actual simulation outputs.

Student Signature : _____

Date : _____

E. Experiment Data Results and Discussion

In Lab Task (During Lab)

Component	Parameter	Value
Input AC Source	Peak-to-peak voltage (Vpp)	
	Frequency (f)	
Operational Amplifier	Power Supply Voltages (+Vcc and −Vcc)	
Resistors	R1	
	R2	
	R3	
	R4	
Capacitors	C_ground	
	C_Vin	
	C_Vout	

Frequency (Hz)	Gain (dB)	Phase Shift (degrees)
10		
100		
1,000		
10,000		
100,000		
1,000,000		

DISCUSSION:

CONCLUSION:

LAB LECTURER
SIGNATURE : _____

DATE : _____

INSTRUCTOR
SIGNATURE : _____

DATE : _____